Remarks/Arguments

The Abstract has been amended to be less than 150 words in length.

Claim 1 has been amended to include the subject matter of claims 2 and 3, and claim 19 has been amended to include the subject matter of claims 21 and 23. The preamble of claim 32 has been amended to direct the claimed invention to dynamic random access memories (DRAM).

Accordingly, claims 2, 3, 21 and 23 have been cancelled from the application, and the dependencies of the remaining claims have been amended where necessary. Claims 4, 13, 34, 40 and 49 have been amended to delete the objected terms “thereto” and “thereof”. Claims 1, 4-20, 22 and 24 to 55 remain pending in the application.

The Examiner rejected claims 1-55 under 35 U.S.C. 102 as being anticipated by the paper titled “An On-chip ECC Circuit for Correcting Soft Errors in DRAM’S with Trench Capacitors”, IEEE Journal of Solid-State Circuits, Vol. 27, No. 11, Nov. 1992, pages 1623-1633, referred to as Mazumder from this point forward.

The Examiner has broadly cited all the figures and all the pages of the Mazumder reference to demonstrate that the recited features of each claim are disclosed. However, the Examiner has not pointed out specific passages of Mazumder nor explained how his interpretation of the Mazumder teachings anticipate the presently claimed features. Applicant has reviewed Mazumder, and now provides amendments and arguments to distinguish the claimed features from Mazumder.

Applicant hereby responds to the Examiner’s rejection to claims 1-55 by addressing individual claim groupings 1-18, 19-31, 32-42 and 43-55.

Claims 1-18

In response to the Examiner’s rejection to claims 1-18 under 35 U.S.C. 102, Applicant has amended claim 1 to include the subject matter of claims 2 and 3, and submits that the subject matter of claims 2 and 3 are not described nor disclosed in Mazumder.

More specifically, amended claim 1 now recites an error detection system for a memory having a memory block, a row parity circuit and a local data I/O circuit. The local data I/O circuit couples a data word from the memory block to global datalines, and provides a row parity bit stored in the memory block. The row parity circuit is now recited to include a serial parity chain for providing a parity output corresponding to a parity of the data word, and a

sense circuit for receiving the parity output from the serial parity chain and the row parity bit, for providing a local parity fail flag if the logic state between the parity output and the row parity bit mismatch.

Applicant submits that Mazumder does not teach, describe or infer a row parity circuit having:

1) a serial parity chain for providing a parity output corresponding to a parity of the data word; and

2) a sense circuit for receiving the parity output from the serial parity chain and the row parity bit for providing a local parity fail flag.

In the present application, an embodiment of the row parity circuit is shown in Figures 5 and 6, and described at paragraph [0069] of the description. Paragraph [0069] describes how each bit of the data word is used to generate even or odd parity signals in the serial parity chain, which are then compared to the row parity bit by the sense circuit.

Mazumder on the other hand only discusses that row parity can be achieved, but does not discuss any circuit implementation which could be considered analogous to the claimed serial parity chain. More specifically, Mazumder does not discuss or show a serial parity chain for generating a parity output to be compared with a row parity bit. Mazumder does not discuss or show a sense circuit for generating a flag by comparing the state of the parity output to the row parity bit. Therefore, Applicant submits that amended claim 1 is not anticipated by Mazumder as Mazumder does not teach, disclose or infer the recited row parity circuit.

Since Mazumder does not describe or disclose a row parity circuit having a serial parity chain and a sense circuit, Applicant submits that further claimed features of the row parity circuit are absent in Mazumder. More specifically, Mazumder does not:

- disclose odd and even parity lines of the serial parity chain, as recited in claim 4;
- disclose a sense circuit of the row parity circuit as including a cross-coupled latch circuit, as recited in claim 5;
- disclose a switching means for coupling the latched parity output to the memory block during a write operation, as recited in claim 6;
- disclose a serial parity chain segmented into at least two serially connected sub-parity circuits, as recited in claim 7.

In conclusion, Applicant submits that amended claim 1 is novel and unanticipated by Mazumder, therefore claims 4-18 by virtue of being dependent on claim 1 either directly or indirectly, are submitted to be unanticipated by Mazumder. Therefore, withdrawal of the Examiner's rejection to claims 1 and 4-18 under 35 U.S.C. 102 is requested.

Claims 19-31

In response to the Examiner's rejection to claims 19-31 under 35 U.S.C. 102, Applicant has amended claim 19 to include the subject matter of claims 21 and 23, and submits that the subject matter of claims 21 and 23 are not described nor disclosed in Mazumder.

More specifically, amended claim 19 now recites a method for detecting and purging errors in a memory by a) executing a read operation to provide a data word onto a local databus, b) comparing row parity of the data word against a row parity bit, c) iteratively multiplexing bits of the data word from the local databus onto a corresponding global databus line for comparing column parity of each bit of the data word with a corresponding column parity word bit in response to row parity failure, and d) inverting bits of the data word when a failed column parity is detected.

Applicant submits that Mazumder does not teach, describe or infer an analagous method where:

1) a read operation is executed for providing a data word onto a local databus and for providing a row parity bit, for row parity comparison; and

2) comparing column parity by iteratively multiplexing bits of the data word from the local data bus onto a global dataline, and comparing column parity of each bit against a bit of a column parity word in response to row parity failure.

In the present application, an embodiment of the method of amended claim 19 is shown in Figure 11, and described beginning at paragraph [0083]. Steps 300 and 302 generally correspond to recited steps a) and b) of amended claim 19, while steps 306, 308, 310 and 312 generally correspond to recited step c) of amended claim 19. Final step 314 generally corresponds to step d) of amended claim 19.

Mazumder on the other hand, only discusses that column parity can be achieved, but does not recite that the row parity is executed by reading the data word onto local databus lines. Furthermore, nowhere does Mazumder disclose or infer that bits of the data word are iteratively multiplexed onto global databus lines for column parity comparison against bits of a

column parity word. While Mazumder teaches that some output is provided from the parity and MUX circuit blocks of the memory arrays shown in Figures 2 and 3, nowhere does Mazumder state or infer that the output is provided onto local databus lines, nor subsequently onto global databus lines as recited in amended claim 19.

Since Mazumder does not describe or disclose the method of reading a data word onto local databus lines, nor of iteratively multiplexing the data word onto global databus lines, Applicant submits that amended claim 19 is not anticipated by Mazumder. Therefore claims 20, 22 and 24-31 by virtue of being dependent on claim 19 either directly or indirectly, are submitted to be unanticipated by Mazumder . Therefore, withdrawal of the Examiner's rejection to claims 19, 20, 22 and 24-31 under 35 U.S.C. 102 is therefore requested.

Claims 32-42

In response to the Examiner's rejection to claims 32-42 under 35 U.S.C. 102, Applicant respectfully disagrees with the Examiner's conclusion, and traverses his anticipation rejection in view of Mazumder as follows.

Claim 32 is directed to an error detection and purging system for a DRAM memory. The system is recited to include a plurality of memory blocks, a local data I/O circuit, a row parity circuit, and a column parity circuit. The memory blocks store data words. The local data I/O circuit transfers the data words from each memory block to global datalines. The row parity circuit is coupled to the local data I/O circuit for executing a row parity check of the data words against corresponding row parity bits. The column parity circuit is coupled to all the local data I/O circuits, and iteratively transfers a bit from each of the data words onto a different global dataline for executing a column parity check against a bit from a column parity word. Upon detection of a column parity failure, data on the global datalines is inverted.

The Applicant now clarifies the recited elements of claim 32 by referring to the analogous features shown in the Figure 4 embodiment of the invention. The elements shown in Figure 4 are introduced in paragraph [0061] of the present application.

The local data I/O circuit is analogous to elements 54, LDB and 58, whose function is described in paragraph [0056]. The row parity circuit is analogous to element 104 associated with each memory block, whose function and relation to the local data I/O circuit is described in paragraph [0063]. The column parity circuit is analogous to elements 106, 107, 108, 112,

114 and 116, whose function and relation to the local data I/O circuit and the global datalines is described in paragraphs [0063] to [0066].

In contrast, Mazumder is limited to discussing the mathematical concept for achieving his desired goal of detecting two concurrent bit errors. As previously mentioned, the Figures shown in Mazumder conceptually show how an output is generated from the MUX and Parity circuit blocks. While these outputs are presumably product codes resulting from logical operations, nowhere does Mazumder describe the specific circuits that produce these product codes. More importantly, nowhere does Mazumder teach, disclose or infer that the local data I/O circuits and the global datalines are used to generate the product codes. In fact, Mazumder does not even describe the use of any local data lines or global datalines. Furthermore, while Mazumder discloses the presence of a multiplexor circuit, nowhere does he describe that it iteratively multiplexes the bits of the data words onto global datalines for executing a column parity check. In conclusion, many elements recited in claim 32 are clearly absent in Mazumder.

Notwithstanding the novelty of claim 32, Applicant submits that the features recited in dependent claims 33-42 are not disclosed in Mazumder. More specifically, dependent claims 33-42 recite specific circuit elements which are not disclosed by Mazumder.

Applicant therefore submits that Mazumder does not disclose the features recited in claim 32, and respectfully requests that the Examiner withdraw his rejection under 35 U.S.C. 102. In view of the novelty of claim 32, Applicant submits that dependent claims 33-42 which depend directly or indirectly from claim 32, must also be novel. Therefore, withdrawal of the Examiner's rejection to claims 32-42 under 35 U.S.C. 102 is requested.

Claims 43-55

In response to the Examiner's rejection to claims 43-55 under 35 U.S.C. 102, Applicant respectfully disagrees with the Examiner's conclusion, and traverses his anticipation rejection in view of Mazumder as follows.

Claim 43 is directed to a method of generating both row and column parity bits when writing a dataword to a memory. An embodiment of the method is shown in Figure 13 and described starting at paragraph [0105].

Applicant submits that Mazumder does not describe a method whereby a dataword at the write address is read out and temporarily stored, followed by writing the new dataword into

the write address and generating the corresponding row parity bit, followed by a comparison of the individual bit positions of the stored dataword and the newly written dataword. Mazumder does not disclose a final step of inverting a column parity bit of a column parity word when the corresponding bit positions of the stored and new dataword mis-match.

Notwithstanding the novelty of claim 43, Applicant submits that the features recited in dependent claims 44-55 are not disclosed in Mazumder. More specifically, dependent claims 44-55 recite specific steps involving circuit elements, both of which are not disclosed by Mazumder.

Applicant therefore submits that Mazumder does not disclose the features recited in claim 43, and respectfully requests that the Examiner withdraw his rejection under 35 U.S.C. 102. In view of the novelty of claim 43, Applicant submits that dependent claims 44-55 which depend directly or indirectly from claim 43, must also be novel. Therefore, withdrawal of the Examiner's rejection to claims 43-55 under 35 U.S.C. 102 is requested.

Summary

In view of the above amendments and remarks, Applicant submits that claims 1, 4-20, 22 and 24-55 are distinguished from Mazumder, and withdrawal of the Examiner's rejection under 35 U.S.C. 102 is respectfully requested.

Should the Examiner disagree with the presented arguments, Applicant invites the Examiner to clarify his rejections based on the Mazumder reference so that a further reply can be submitted to further advance prosecution of this application.

Miscellaneous claim amendments

Applicant takes the opportunity to amend claims 43-45, 47 and 48 to clarify features of the claimed invention.

New dependent claims 56 and 57 have been added to recite that the temporary storage of the data word and the new data word includes latching into data registers.

Applicant submits that no new matter is being introduced the by aforementioned amendments to the claims.

The Commissioner is hereby authorized to debit $120.00 from Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP, representing a one month extension of time fee.

The Commissioner is hereby authorized to charge any additional fees, and credit any over payments to Deposit Account No. 501593, in the name of Borden Ladner Gervais LLP.

Respectfully submitted,

Richard FOSS

/Shin Hung/

By: _____

Shin Hung
Reg. No. 55,497
Borden Ladner Gervais LLP
World Exchange Plaza
100 Queen Street, Suite 1100
Ottawa, ON K1P 1J9
CANADA
Tel: (613) 787-3571
Fax: (613) 787-3558
E-mail: shung@blgcanada.com

SHH/ats
Encls.
1. Extension of Time